DCEL101

Reg. No. | | | | | | | | |

I Semester B.Sc. Degree Examination, May/June- 2022

ELECTRONICS

Electronic Devices & Circuits

(NEP 2020 Scheme)

Paper : ELE -CT1

Time : 2½ Hours | Maximum Marks : 60

Instructions to Candidates:

Answer all the questions from Part -A, any FOUR questions from Part-B and any FOUR questions from Part -C

Note: Answer all the questions of Part-A in any one page and to be answered only once. In this Part, answering the same question multiple times will not be considered for Evaluation.

PART - A

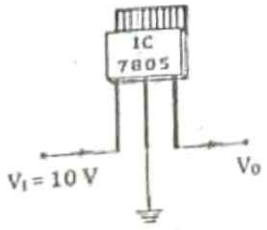
1. Answer **All** the Sub divisions (12×1=12)

i) The circuit whose properties are same in either direction is known as
   a) Unilateral circuit b) Bilateral circuit
   c) Irreversible circuit d) Reversible circuit

ii) For maximum transfer of power, internal resistance of the source should be
   a) equal to load resistance b) Less than load resistance
   c) Greater than load resistance d) None of the above

iii) Theoretical value of efficiency for a full Wave Rectifier is
   a) 40. 6% b) 81.2%
   c) 21.0% d) 1.21%

iv) Output voltage in the following circuit is
   a) 10 V b) 5V
   c) -10V d) -5 V



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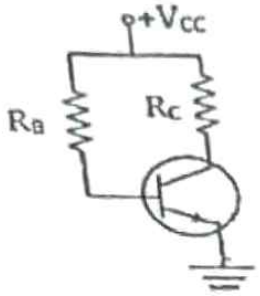
v) The transistor gets the name BJT as the conduction is
   a) Due to immobile ions.
   b) Due to only holes
   c) Due to both holes and electrons.
   d) Due to only electrons.

vi) The correct relationship between the two current gains in BJT is
   a) $\alpha = \beta / 1 + \beta$
   b) $\alpha = 1 - \beta$
   c) $\alpha = \beta / 1 - \beta$
   d) $\alpha = \beta + 1$

vii) The biasing circuit shown in figure is
   a) Collector to base bias
   b) Voltage divider bias
   c) Emitter bias
   d) Fixed bias



viii) Common collector amplifier is always used as
   a) Voltage amplifier
   b) Power amplifier
   c) Impedance matching amplifier
   d) audio amplifier

ix) What is the input voltage of an amplifier with gain of 50 to generate 10V output?
   a) 1 V
   b) 200mV
   c) 1mV
   d) 200V

x) Which segments of a seven segment display need to be active in order to display a decimal digit 9 ?
   a) a, c, d, e, f
   b) a, b, e, f, g
   c) a, b, c, d, f,g
   d) c, d, e, f

xi) The BCD code for decimal number 10 is
   a) 1000 0000
   b) 0101 0000
   c) 0000 1010
   d) 0001 0000

xii) _____ is a derived logic gate.

a) OR gate b) XOR gate
c) NOT gate d) AND gate

PART - B

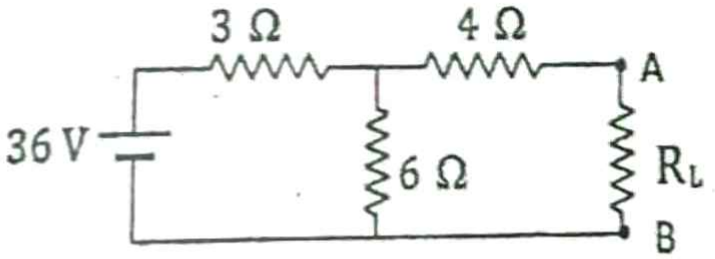
Answer any **Four** questions. (4×7=28)

2. a) State Thevenin's theorem. With suitable circuit diagrams, explain the steps to Thevenise a resistive network.
   b) Draw the input and output waveforms of HWR. (5+2)
3. a) Draw the block diagram of a regulated power supply and explain each block.
   b) What are voltage multipliers? (5+2)
4. a) Explain the input and output characteristic curves for a transistor in CE mode.
   b) Establish the relation between β and γ for a transistor. (5+2)
5. With a circuit diagram, explain the working of a two stage RC coupled CE amplifier and draw its frequency response. (7)
6. a) Explain with numerical example, method to convert a decimal number into Binary and Hexadecimal equivalent.
   b) Convert binary number $111010101_{(2)}$ into Gray code equivalent. (5+2)
7. a) State and prove De Morgan's theorems.
   b) Verify the universal property of NOR gate by realizing AND gate. (5+2)

PART - C

Answer any **Four** questions. (4×5=20)

8. Find the current through load resistor $R_L = 12\ \Omega$ using Norton's theorem. (5)



9. Calculate efficiency and PIV of a FWR with an input voltage of 230V rms and load resistance of 100 Ω. Given $r_d = 5\ \Omega$ and turns ratio 10:1. (5)

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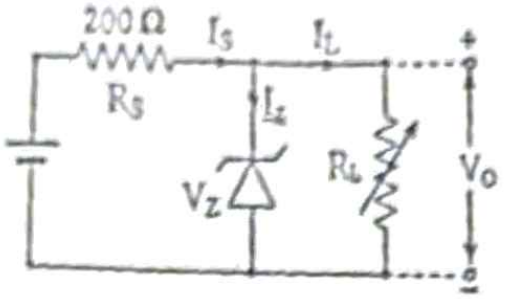
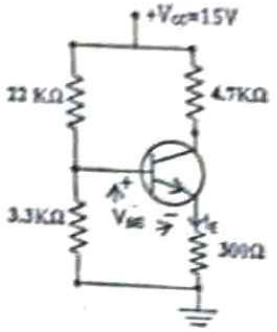
10. Calculate Iz (min) and Iz (max) in the circuit shown. Given: Vz=10V, Vin=36V and PZ = 500mW. (5)



11. Draw the DC load line and mark the operating point for the biasing circuit shown in figure using Silicon transistor. Given β=200. (5)



12. a) Subtract 20H from 5EH using 2's complement method.
    b) Add $10111_{(2)}$ and $11010_{(2)}$ express the result in decimal. (3+2)

13. Simplify the Boolean expression $Y = [A\overline{B}(C + AD) + \overline{A}\overline{B}]C$ and realise using basic gates. (5)